Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (original) An integrated circuit design system comprising:

a second interface for displaying a plurality of description instructions corresponding to an application-specific integrated circuit (ASIC) according to a variety of display instructions;

a first interface for inputting the display instructions and for updating the description instructions displayed on the second interface according to the display instructions; and

a logic unit for updating any description instruction but an updated description updated by the first interface corresponding to the ASIC according to the updated description instruction.

2. (original) The integrated circuit design system of claim 1, wherein the plurality of description instructions comprises a timing slack report of the ASIC.

3. (original) The integrated circuit design system of claim 1, wherein the plurality of description instructions comprises a netlist of the ASIC.

4. (original) The integrated circuit design system of claim 1, wherein the plurality of description instructions comprises a noise analysis report of the ASIC.

5. (original) The integrated circuit design system of claim 1, wherein the plurality of description instructions comprises a power analysis report of the ASIC.

6. (currently amended) The integrated circuit design system of claim 3, wherein the logic unit is further capable of calculating a noise analysis report corresponding

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to an ~~undated~~updated netlist.

7. (currently amended) The integrated circuit design system of claim 3, wherein the logic unit is further capable of calculating a power analysis report corresponding to an ~~undated~~updated netlist.

8. (currently amended) The integrated circuit design system of claim 3, wherein the logic unit is further capable of calculating a timing slack report corresponding to an ~~undated~~updated netlist.

9. (original) The integrated circuit design system of claim 1, wherein the logic unit is further capable of executing a clock tree synthesis.

10. (original) The integrated circuit design system of claim 1, wherein the logic unit is further capable of executing a timing optimization process.

11. (original) The integrated circuit design system of claim 1, wherein the logic unit is further capable of executing a cell & wire extraction process and for generating a cell & wire delay of a standard delay format (SDF).

12. (original) The integrated circuit design system of claim 1, wherein the second interface is capable of displaying cells and interconnects connected between the cells of the ASIC according to a specified display instruction input to the first interface.

13. (original) The integrated circuit design system of claim 12, wherein the second interface is capable of further displaying spare cells neighboring the cells according to the specified display instruction.

14. (original) The integrated circuit design system of claim 12, wherein the second interface is capable of displaying a plurality of specified icons, each of the icons corresponding to a specified cell having a specified function corresponding to the

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specified icon.

15. (original) The integrated circuit design system of claim 2, wherein the logic unit is further capable of dividing the timing slack report into a plurality of timing slack sub-reports, each of the timing slack sub-reports having less information than that of the timing slack report.

16. (original) The integrated circuit design system of claim 15, wherein the logic unit divides the timing slack report into the timing slack sub-reports according to circuit components referenced by the timing slack report.

17. (original) The integrated circuit design system of claim 15, wherein the logic unit divides the timing slack report into the timing slack sub-reports according to clocks referenced by the timing slack report.

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